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PATENTS

Attorney Docket No.: ELM-2 Cont. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Glenn J. Leedy
Application No. : 10/672,961 Confirmation No.: 9439
Filed : September 26, 2003
For : THREE DIMENSIONAL MULTI LAYER MEMORY AND
CONTROL LOGIC INTEGRATED CIRCUIT
STRUCTURE (AS AMENDED)
Art Unit : 2822
Examiner : Monica Lewis

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicant wishes to call the attention of the Examiner to the
following documents:

U.S. Patent Documents

Sobczak	08-05-1986	US 4,604,162
Butt et al.	07-18-1989	US 4,849,857
Williamson	05-22-1990	US 4,928,058
Sliwa	02-05-1991	US 4,990,462
Kessler et al.	05-05-1992	US 5,110,712
Sliwa et al.	06-02-1992	US 5,119,164
Moslehi	02-08-1994	US 5,284,804
Clifton et al.	01-02-1996	US 5,480,842
Sachdev et al.	11-28-1995	US 5,470,693

12/28/2005 HLE333 00000100 061075 10672961

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U.S. Patent Documents

Bair et al.	11-19-1996	US 5,577,050
Di Zenzo et al.	04-28-1998	US 5,745,673
Bertin et al.	10-06-1998	US 5,818,748
Flesher et al.	03-31-1998	US 5,733,814
Clifton et al.	04-09-2002	US Re 37,637

Foreign Patent Documents

EP 0 201 380	B1	12-17-1986	Fairchild Semiconductor Corporation
EP 0 224 418	B1	06-03-1987	Fujitsu Limited
EP 0 419 898	B1	04-03-1991	Siemens Aktiengesellschaft
EP 0 455 455	B1	11-06-1991	AT&T Corp.
EP 0 487 302	B1	05-27-1992	Shin-ETSU Handotai Company Limited
EP 0 503 816	B1	09-16-1992	Shin-ETSU Handotai Company Limited
EP 0 518 774	B1	12-16-1992	France Telecom
EP 0 526 551	B1	02-10-1993	The Commonwealth of Australia
EP 0 554 063	B1	08-04-1993	Canon Kabushiki Kaisha
EP 0 555 252	B1	08-18-1993	Fraunhofer-Gesellschaft Zur Förderung Der Angewandten Forschung E.V..
WO 1989 010255		11-02-1989	3D Systems Inc.
WO 1990 009093		08-23-1990	Polyolithics Inc.
WO 1992 017901		10-15-1992	Integrated System Assemblies Corporation

Nonpatent Literature Documents

Jones, R.E., Jr. "An evaluation of methods for passivating silicon integrated circuits"; April 1972; pp. 23-8

Svechnikov, S.V.; Kobyl'yatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminum membrane crossings of conductors"; 1972

Nonpatent Literature Documents

Sun, R.C.; Tisone, T.C.; Cruzan, P.D.; "Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)"; March 1973; pp. 1009-16

Wade, T.E.; "Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection"; 1982; pp. 516-19

Boyer, P.K.; Collins, G.J.; Moore, C.A.; Ritchie, W.K.; Roche, G. A.; Solanski, R. (A); Tang, C.C.; "Microelectronic thin film deposition by ultraviolet laser photolysis MONOGRAPH TITLE - Laser processing of semiconductor devices"; 1983; pp. 120-126

Boyer, P.K.; Moore, C.A.; Solanki, R.; Ritchie, W.K.; Roche, G.A.; Collins, G.J.; "Laser photolytic deposition of thin films"; 1983; pp. 119-27

Chen, Y.S.; Fatemi, H.; "Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits"; May-June 1986; pp. 645-9

Salazar, M.; Wilkins, C.W., Jr.; Ryan, V.W.; Wang, T.T.; "Low stress films of cyclized polybutadiene dielectrics by vacuum annealing"; Oct. 21-22, 1986; pp. 96-102

Townsend, P.H.; Huggins, R.A.; "Stresses in borophosphosilicate glass films during thermal cycling"; Oct. 21-22, 1986; pp. 134-41

Pai, Pei-Lin; "Multilevel Interconnection Technologies--A Framework And Examples"; 1987; pp. 1871

Pei-lin Pai; Chetty, A.; Roat, R.; Cox, N.; Chiu Ting; "Material characteristics of spin-on glasses for interlayer dielectric applications"; November 1987, pp. 2829-34

Allen, Mark G.,; Senturia, Stephen D.; "Measurement of polyimide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356

Chang, E.Y.; Cibuzar, G.T.; Pande, K.P.; "Passivation of GaAs FET's with PECVD silicon nitride films of different stress states"; September 1988; pp. 1412-18

Riley, P.E.; Shelley, A.; "Characterization of a spin-applied dielectric for use in multilevel metallization"; May 1988; pp. 1207-10

Nonpatent Literature Documents

Tamura, H.; Nishikawa, T.; Wakino, K.; Sudo, T.;
"Metalized MIC substrates using high K dielectric
resonator materials"; October 1988; pp. 117-126

Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I.
Kalinin Leningrad Polytechnic Institute (USSR);
"Electrophysical investigation of thin-layered
inorganic coatings"; 1989; pp. 826-828

Reche, J.J. H.; "Control of thin film materials
properties used in high density multichip
interconnect"; April 24-28, 1989; p. 494

Maw, T.; Hopla, R.E.; "Properties of a photoimageable
thin polyimide film"; Nov. 26-29-, 1990; pp. 71-6

Draper, B. L.; Hill, T.A.; "Stress and stress
relaxation in integrated circuit metals and
dielectrics"; July-Aug. 1991; pp. 1956-62

Guckel, H.; "Surface micromachined pressure
transducers"; 1991; pp. 133-146

Garino, T.J.; Harrington, H. M.; "Residual stress in
PZT thin films and its effect on ferroelectric
properties'; 1992; pp. 341-7

The aforementioned references are listed on the
accompanying Form PTO-SB/08 (submitted in duplicate).
Pursuant to 37 C.F.R. § 1.98 (a)(2), no copies of the
aforementioned U.S. Patent Documents are being submitted.
Copies of the listed Foreign Patent Documents and Nonpatent
Literature Documents are being submitted herewith.

Applicant reserves the right to establish the
patentability of the claimed invention over any of the
information provided herewith, and/or to prove that this
information may not be prior art, and/or to prove that this
information may not be enabling for the teachings purportedly
offered.

It is respectfully requested that these references
be: (1) fully considered by the Patent and Trademark Office
during the examination of this application; and (2) printed on

any patent which may issue on this application. Applicant requests that a copy of Form PTO-SB/08, as considered and initialled by the Examiner, be returned with the next communication.

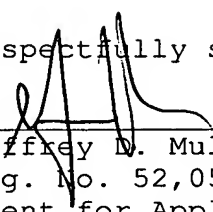
The Clifton and Flesher U.S. Patent Documents (U.S. Patent Nos. 5,480,842, 5,733,814, and Re 37,637) were cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/614,067 on September 21, 2005. Butt et al. U.S. Patent No. 4,849,857 was cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/971,341 on September 20, 2005. Bair et al. U.S. Patent No. 5,577,050, Bertin et al. U.S. Patent No. 5,818,748, and Di Zenzo et al. U.S. Patent No. 5,745,673 were cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/143,200 on October 18, 2005.

The remaining references cited in this Information Disclosure Statement were brought to applicant's attention in a third-party search. A copy of the third-party search results is enclosed herewith.

This Supplemental Information Disclosure Statement is being submitted after the mailing of a first office action on the merits. Accordingly, the director is authorized to charge \$180.00, in accordance with 37 C.F.R. § 1.97(c) to Account No. 06-1075, Order No. 001202-0002. A duplicate copy of this document is being submitted herewith.

An early and favorable action is respectfully
requested.

Respectfully submitted,



Jeffrey D. Mullen
Reg. No. 52,056
Agent for Applicant
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020-1105
Tel.: (212) 596-9000
Fax: (212) 596-9090



PTO/SB/08a/b (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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Substitute for form 1449A/B/PTO				Complete if Known	
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/672,961
				Filing Date	September 26, 2003
				First Named Inventor	Glenn J. Leedy
				Art Unit	2822
				Examiner Name	Monica Lewis
Sheet	1	of	3	Attorney Docket Number	ELM-2 Cont. 4

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US 4,604,162	08-05-1986	Sobczak	
		US 4,849,857	07-18-1989	Butt et al.	
		US 4,928,058	05-22-1990	Williamson	
		US 4,990,462	02-05-1991	Sliwa	
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		US 5,119,164	06-02-1992	Sliwa et al.	
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		US 5,470,693	11-28-1995	Sachdev et al.	
		US 5,733,814	03-31-1998	Flesher et al.	
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		EP 0 201 380 B1	12-17-1986	Fairchild Semiconductor Corporation		
		EP 0 224 418 B1	06-03-1987	Fujitsu Limited		
		EP 0 419 898 B1	04-03-1991	Siemens Aktiengesellschaft		
		EP 0 455 455 B1	11-06-1991	AT&T Corp.		
		EP 0 487 302 B1	05-27-1992	Shin-ETSU Handotai Company Limited		
		EP 0 503 816 B1	09-16-1992	Shin-ETSU Handotai Company Limited		
		EP 0 518 774 B1	12-16-1992	France Telecom		
		EP 0 526 551 B1	02-10-1993	The Commonwealth of Australia		
		EP 0 554 063 B1	08-04-1993	Canon Kabushiki Kaisha		
		EP 0 555 252 B1	08-18-1993	Fraunhofer-Gesellschaft Zur Förderung Der Angewandten Forschung E.V..		
		WO 1989 010255	11-02-1989	3D Systems Inc.		
		WO 1990 009093	08-23-1990	Polyolithics Inc.		
		WO 1992 017901	10-15-1992	Integrated System Assemblies Corporation		

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				Examiner Name	Monica Lewis
Sheet	2	of	3	Attorney Docket Number	ELM-2 Cont. 4

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Jones, R.E., Jr. "An evaluation of methods for passivating silicon integrated circuits"; April 1972; pp. 23-8	
		Svechnikov, S.V.; Koblyatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminum membrane crossings of conductors"; 1972	
		Sun, R.C.; Tisone, T.C.; Cruzan, P.D.; "Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)"; March 1973; pp. 1009-16	
		Wade, T.E.; "Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection"; 1982; pp. 516-19	
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		Chen, Y.S.; Fatemi, H.; "Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits"; May-June 1986; pp. 645-9	
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		Chang, E.Y.; Cibuzar, G.T.; Pande, K.P.; "Passivation of GaAs FET's with PECVD silicon nitride films of different stress states"; September 1988; pp. 1412-18	
		Riley, P.E.; Shelley, A.; "Characterization of a spin-applied dielectric for use in multilevel metallization"; May 1988; pp. 1207-10	
		Tamura, H.; Nishikawa, T.; Wakino, K.; Sudo, T.; "Metalized MIC substrates using high K dielectric resonator materials"; October 1988; pp. 117-126	
		Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828	
		Reche, J.J. H.; "Control of thin film materials properties used in high density multichip interconnect"; April 24-28, 1989; p. 494	

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				Examiner Name	Monica Lewis
Sheet	3	of	3	Attorney Docket Number	ELM-2 Cont. 4

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Maw, T.; Hopla, R.E.; "Properties of a photoimageable thin polyimide film"; Nov. 26-29-, 1990; pp. 71-6	
		Draper, B. L.; Hill, T.A.; "Stress and stress relaxation in integrated circuit metals and dielectrics"; July-Aug. 1991; pp. 1956-62	
		Guckel, H.; "Surface micromachined pressure transducers"; 1991; pp. 133-146	
		Garino, T.J.; Harrington, H. M.; "Residual stress in PZT thin films and its effect on ferroelectric properties"; 1992; pp. 341-7	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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